

REMARKS

No substitute specification being submitted.

No new matter has been added.

The Examiner is requested to call the undersigned if any questions arise concerning the above-mentioned application.

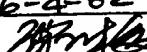
Respectfully submitted,

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I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
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ON 6-4-02


VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the paragraph on page 4 line 15 to line 28 with the followings:

The interface board 29 can be used simply to reverse the arrangement of the connector pins, or it can be designed to serve other functions as well. For example, it can be used to create a test environment for the semiconductor devices (in this example, memory devices) within the sockets 31 which are actual operating conditions that the devices might encounter on the circuit board. That is, the interface board 29 can be designed to compensate for the environmental differences caused by use of the sockets 31, as well as the use of additional equipment that might be added. An example of such an interface board is disclosed in Korean Patent Application No. 2000-20653 entitled "Interface Board And Test Method For Semiconductor Integrated Circuit Devices Using The Same." which is incorporated by reference, and U.S. Patent Application Ser. No. 09/733,336 filed December 08, 2000 entitled "Method And Apparatus For Testing Semiconductor Devices Using An Actual Board-Type Product" which is incorporated by reference. For example, this compensation can include the control of the clock signal timing, the control of the signal timing margin, the control of AC signal parameters, and the control of the power supply signals.